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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/675,815	09/28/2000	Gregory A. Overkamp	10559/274001/P9281-ADI	9785

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EXAMINER	
TSAI, HENRY	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/675,815	OVERKAMP ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2005* .

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,4-15,17,18 and 23-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,4-15,17,18 and 23-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ___ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "loading the plurality of instructions into a **register**, said plurality of instructions including two or more instructions received from different ones of a plurality of instruction sources" (in claims 9, and 14); and "an instruction size determination unit, producing instruction sizes respectively associated with said plurality of instruction sources" (in claim 25) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Note Fig. 5 shows a plurality of instruction sources, 505, 510, 515, and 520. However, it does not show **a register** receiving instructions from the instruction sources and there's no **instruction size determination unit** shown.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 2, 4-15, 17, 18 and 23-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In claim 9, lines 7-9, it is not clear what is meant by "instruction sources are each associated with **a different location in an instruction pipeline**" since "**a different location in an instruction pipeline" was not described.**

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 2, 4-15, 17, 18 and 23-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 9, lines 7-9, the term, "a different location in an instruction pipeline" lacks proper antecedent basis since it was previously not defined. Similar problems exist in the other claims 14, 23, and 25.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of

> section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 9, 13-15, 17, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Favor et al. (U.S. Patent No. 5,809,273) (Hereafter referred to as Favor et al.'273).

Referring to claim 9, Favor et al.'273 discloses, as claimed, a method of decoding a plurality of instructions within a processor (microprocessor 120, See Fig. 1) comprising: determining the size of the plurality of instructions (see Col. 10, lines 30-32, regarding predecoder unit 203 decodes the instruction bytes to determine the number of instructions and length of each instruction); loading the plurality of instructions into an instruction register (instruction cache

214, see Fig. 2, note the instruction cache 214 is best reasonably and broadly interpreted as a register since it is a fast storage device saving the instructions), said plurality of instructions including two or more instructions received from different ones of a plurality of instruction sources (main memory 120 and L2 cache 122, see Fig. 1 since at least both of them provide instruction inputs to instruction cache 214, see Figs. 1 and 2);

Wherein the plurality of instruction sources are each associated with a different location (best reasonably and broadly interpreted as "stage") in an instruction pipeline (since the instructions in instruction cache 214 from main memory 120 and L2 cache 122, are fetched at different stages in an instruction pipeline);

presenting the plurality of instructions from the instruction register (instruction cache 214, see Fig. 2, note the instruction cache 214 is best reasonably and broadly interpreted as a register since it is a fast storage device saving the instructions) to a decoder (instruction decoder 220, see Fig. 2); and decoding (by such as instruction decoder 220, see Fig. 2, and col. 3, lines 25-27, regarding instructions are decoded in parallel) each of the plurality of instructions

within a single clock cycle (see col. 3, lines 19-21, regarding multiple instructions are decoded per cycle).

Referring to claim 14, Favor et al.'273 discloses, as claimed, a processor (microprocessor 120, See Fig. 1) comprising: an instruction register (instruction cache 214, see Fig. 2, note the instruction cache 214 is best reasonably and broadly interpreted as a register since it is a fast storage device saving the instructions) capable of holding a plurality of instructions, said plurality of instructions including two or more instructions received from different ones of a plurality of instruction sources (main memory 120 and L2 cache 122, see Fig. 1 since at least both of them provide instruction inputs to instruction cache 214, see Figs. 1 and 2); Where the plurality of instruction sources are each associated with a different location (best reasonably and broadly interpreted as "stage") in an instruction pipeline (since the instructions in instruction cache 214 from main memory 120 and L2 cache 122, are fetched at different stages in an instruction pipeline);

one or more pre-decoders (predecoder 270, see Fig. 2) which determines the size and number of the plurality of instructions (see Col. 5, lines 43-49, regarding predecoder 270 decodes the instruction bytes to determine the length of each instruction and therefore the number of instructions once the instruction

boundaries are known); and a decoder (instruction decoder 220, see Fig. 2, and col. 3, lines 25-27, regarding instructions are decoded in parallel) which substantially simultaneously receives the plurality of instructions from the instruction register (see col. 3, lines 25-27, regarding instructions are decoded in parallel), wherein the decoder decodes each of the plurality of instructions within a single clock cycle (see col. 3, lines 19-21, regarding multiple instructions are decoded per cycle).

As to claims 13, and 18, Favor et al.'273 also discloses: handling the plurality of instructions within a digital signal processor (microprocessor 120, See Fig. 1).

As to claim 15, Favor et al.'273 also discloses: decoding the plurality of instructions to determine the width of the plurality of instructions (see Col. 5, lines 43-49, regarding predecoder 270 decodes the instruction bytes to determine the length of each instruction and therefore the number of instructions once the instruction boundaries are known).

As to claim 17, Favor et al.'273 also discloses: the pre-decoder (predecoder 270, see Fig. 2) communicates the number and size of the plurality of instructions to the decoder (see Col. 5, lines 34-40, regarding predecoder unit 270 decodes the instruction bytes to determine the number of instructions and

length of each instruction and transfer the predecode information to decoder 220).

8. Claims 2, 4-9, 10-12, 23 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Fleck et al. (U.S. Patent No. 6,292,845) (Hereafter referred to as Fleck et al.'845).

Referring to claim 23, Fleck et al.'845 discloses as claimed a method, comprising: receiving (from instruction buffer 3 see Fig. 1) instructions (see Fig. 3A and Fig. 3B) and size information (from 35a, 35b, and 35c see Fig. 1, see also col. 4, line 67, and col. 5, lines 1-3) associated with the instructions from a plurality of different instruction sources (such as internal cache memories and external memories in the Fleck et al.'845's system. Note the saved instructions in memory 1 can be from different instruction sources.), into a switching part (Multiplexer 4, see Fig. 1), each instruction source associated with a different location in an instruction pipeline (see Col. 1, line 57); and using the switching part (Multiplexer 4, see Fig. 1) to switch among the instruction sources (since as set forth the saved instructions in memory 1 can be from different instruction sources), said using providing an instruction and associated size information (the 16-bit size or 32-bit size, see Fig. 3A and Fig. 3B) at an output (16 bits each see Fig. 1)

thereof; receiving the output from the switching part into a decoder (8 or 9 see Fig. 1); and using the decoder (8 or 9 see Fig. 1) to decode each instruction, using said associated size information (the 16-bit size or 32-bit size, see Fig. 3A and Fig. 3B).

As to claim 2, Fleck et al.'845 also discloses: decoding the plurality of instructions within a single clock cycle (see Fig. 1 and col. 3, lines 37-52, regarding the instructions are decoded in parallel).

As to claim 4, Fleck et al.'845 also discloses: decoding (by instruction length and type evaluation 7, see Fig. 1) width bits (35a-c, see Fig. 1) to determine the size of the instructions.

As to claim 5, Fleck et al.'845 also discloses: where a number of simultaneous instructions is greater than 1 (see Fig. 1, there can be four simultaneous 16-bit instructions), and communicating the number and size of the plurality of instructions to the decoder (8 and 9, see Fig. 1).

As to claim 6, Fleck et al.'845 also discloses: loading a first of the plurality of instructions having a first size (16-bit size, see col. 3, lines 37-52) and a second of the plurality of instructions having a second size (32-bit size, see col. 3, lines 37-52).

As to claim 7, Fleck et al.'845 also discloses: loading a first of the plurality of instructions having a first size (32-bit size, see col. 3, lines 37-52), and loading a second and a third of the plurality of instructions having a second size (16-bit size, see col. 3, lines 37-52), wherein the first size is 32-bits and the second size is 16-bits.

As to claim 8, Fleck et al.'845 also discloses: handling the plurality of instructions within a digital signal processor (32-bit microprocessor, See col. 2, line 42 and Fig. 1).

As to claim 10, Fleck et al.'845 also discloses: simultaneously presenting each of the plurality of instructions (see Fig. 1, there can be two simultaneous 16-bit instructions) to the decoder (decode L.S 8, or decode integer 9, see Fig. 9).

As to claim 11, Fleck et al.'845 also discloses: pre-decoding (using instruction length and type evaluation 7 see Fig. 1) the plurality of instructions to determine the width of the plurality of instructions.

As to claim 12, Fleck et al.'845 also discloses: loading (from memory 1 see Fig. 1) a next plurality of instructions into the single instruction register (instruction buffer 3, see Fig. 1).

As to claim 24, Fleck et al.'845 also discloses: receiving instructions (see Fig. 3A and Fig. 3B) comprises receiving a

plurality of instruction simultaneously and size (from 35a, 35b, and 35c see Fig. 1, see also col. 4, line 67, and col. 5, lines 1-3) associated with said plurality of instructions (see Fig. 1, there can be two simultaneous 16-bit instructions), and decoding (by decoder 8 or 9, see Fig. 1) the plurality of instructions substantially simultaneously.

Allowable Subject Matter

9. Claims 25 and 26 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

10. The following is a statement of reasons for the indication of allowable subject matter: Fleck et al. (U.S. Patent No. 6,292,845), the closest reference, and the other prior art do not teach or fairly suggest: in additional to a first switching element, a second switching element which switches sizes from the instruction size determination unit (in claim 25). Further, the combination of the limitations with all of the other limitations in claim 25 is not obvious.

Response to Arguments

11. Applicant's arguments mailed 4/26/05 have been considered but are moot in view of the new ground(s) of rejection.

Regarding the drawings problems, Applicant's response has not completely overcome the objections. Regarding Fig. 5, Applicants argue that a multiplexer 525 is used to represent a **register**. Examiner disagrees with Applicants since it is well known in the art that a multiplexer is used to select an output from a plurality of inputs; and a register is used to temporarily save a data. They provide different functions.

Applicants further argue that "Claim 23, for example, defines that each instruction source is "associated with a different location in an instruction pipeline". Favor et al teaches nothing about this subject Favor et al teaches nothing about this subject matter; in fact, the interpretation of the present claims uses main memory 112, and 12 cache 122 as the instruction sources. This is certainly not associated with multiple locations in a pipeline, as claimed" (page 9, last paragraph and page 10, lines 1-2). Examiner disagrees with Applicants. As set forth in the 112, 2nd rejections, it is not clear what is meant by "instruction sources are each associated

with a different location in an instruction pipeline" since "a different location in an instruction pipeline" was not defined. As set forth in the art rejections above, Favor et al.'273 discloses the plurality of instruction sources being each associated with a different location (best reasonably and broadly interpreted as "stage") in an instruction pipeline (since the instructions in instruction cache 214 from main memory 120 and L2 cache 122, are fetched at different stages in an instruction pipeline).

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened

statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to **the TC central telephone number, 571-272-2100.**

14. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions

directly into **the Group at fax number: 703-872-9306.** This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

June 9, 2005